

# UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,235	04/22/2004	Takashi Ohtsuka	63979-042	7116
7	7590 10/15/2004		EXAMINER	
	T, WILL & EMERY		LE, THON	G QUOC
600 13th Street Washington, D	i, N.W. OC 20005-3096		ART UNIT	PAPER NUMBER
-			2818	<u>-</u>
			DATE MAILED: 10/15/2004	1

Please find below and/or attached an Office communication concerning this application or proceeding.

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## Office Action Summary    10/829,235
Thong Q. Le  - The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply  A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above, the maximum statutory period will apply and will expert SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (50 J.C.C. § 135). Any, reply reached by the Order Bet 40 me armine after the mailing date of this communication, even if timely filed, may reclude any examed patient term adjustment. See 37 CFR 1.704(b).  Status  1) Responsive to communication(s) filed on
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A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ② MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after Short (No. 1974) specified above is best than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (a) MONTHON the mailing date of this communication.  Failure to reply within the set or extended period for reply will by statute, cause the application to become ABANDONED (35 U.S. €, \$133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).  Status  1)  Responsive to communication(s) filed on
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11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.
Priority under 35 U.S.C. § 119
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a)⊠ All b)□ Some * c)□ None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No
3. Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
Attachment(s)
1) Notice of References Cited (PTO-892)  4) Interview Summary (PTO-413)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  3) Notice of Draftsperson's Patent Drawing Review (PTO-948)  Paper No(s)/Mail Date  Notice of Informal Patent Application (PTO-152)
Paper No(s)/Mail Date 6) Other:

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#### **DETAILED ACTION**

1. Claims 1-19 are presented for examination.

### Information Disclosure Statement

- This office acknowledges receipt of the following items from the Applicant:
   Information Disclosure Statement (IDS) filed on April 22, 2004.
- 3. Information disclosed and list on PTO 1449 was considered.

## **Priority**

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

#### Specification

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

# Claim Rejections - 35 USC § 112

- 6. The following is a quotation of the second paragraph of 35 U.S.C. 112:
  - The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 7. Claims 3, 8,15 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such

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omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: third and fourth inverters, fifth, sixth transistors. etc... Because this claim depends from independent claim 1, which does not teach any transistor or resistor. More specification, this claim disclosed a latch and latch divided in two parts as in Figure 3, INV3, INV 4, and each INV has a transistor and a resistor only. Therefore, claim has to use the number in order. Since invention in Figure 3 is differenced from Figure 2, and it is not relate with invention in Figure 2. Therefore, the name of element in Figure 3 must being independent from claim 2. The name of elements in claim 3 is look like relative with claim 2. It is unclearly.

Claims have to amend for more clearly.

#### Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
- 9. Claims 1, 6, 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Brouwer et al. (U.S. Patent No. 5,936,879)

Regarding claims 1, 6, 13, Brouwer et al. disclose anon-volatile memory cell (Figure 2) comprising:

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a latch circuit (Figure 2) which comprises a first node and a second node and latches complementary data set in the first node and second node (Figure 2, ABSTRACT);

a first switching element (11) which connects the first node to a first data input/output line (Data);

a second switching element (12) which connects the second node to a second data input/output line (/Data);

a first ferroelectric capacitor (17) which connects the second data input/output line to the first node; and

a second ferroelectric capacitor (16) which connects the first data input/output line to the second node.

10. Claims 2,7,14 are rejected under 35 U.S.C. 102(b) as being anticipated by Eliason et al. (U.S. Patent No. 6,141,237)

Regarding claim 2, 7,14, Eliason et al. disclose a non-volatile memory cell (Figure 2) in which the latch circuit comprises

a first inverter (m0, m1) and a second inverter (m2,m3);

the first inverter comprising a first transistor (m0) and a second transistor (m1) which complement each other and are serially connected between a power line (vddp) and ground (Figure 2);

the second inverter comprising a third transistor (m2) and a fourth transistor (m3) which complement each other and are serially connected between the power line (vddp) and ground (Figure 2);

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the first and second transistors each having a the first and second the first node and the transistors being connected gate and a drain, the gates of transistors being connected to drains of the first and second to the second node (Figure 2); and

the third and gate and a drain and fourth transistors each having a the gates of the third and fourth transistors being connected to the second node and the drains of the third and fourth transistors being connected to the first node (Figure 2, ABSTRACT).

#### Allowable Subject Matter

11. Claims 4-5,9-12,16-19 are allowed.

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Claims 4-5,9-12,16-19 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Brouwer et al. (U.S. Patent No. 5,936,879), Eliason et al. (U.S. Patent No. 6,141,237), and others, does not teach the claimed invention having a method of controlling a non-volatile including a recall step including the RECALL step comprising a first substep and a second substep; the first substep comprising setting the potential of a power line of the latch circuit to a ground potential. setting the potentials of the first and second data input/output lines to the ground potential and turning on the first and second switching elements; the second substep, which follows the first substep, comprising, in the state that the potentials of the first and second data input/ output lines are maintained at the ground potential, turning off the first and second switching elements and increasing the potential of the power line of the latch circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le Primary Examiner Art Unit 2818 Page 6

THONG LEI
PRIMARY EXAMINER